REMARKS

In the Office Action, the Examiner noted that claims 1-20 are pending in the application and that claims 1-20 are rejected. By this response, claims 1-20 continue without amendment. In view of the following discussion, Applicants submit that none of the claims now pending in the application are anticipated under the provisions of 35 U.S.C. §102 or obvious under the provisions of 35 U.S.C. §103. Thus, Applicants believe that all of these claims are now in condition for allowance.

I. Rejection Of Claims Under 35 U.S.C. §102

The Examiner rejected claims 1-2, 4, 6-8, and 11-20 as being anticipated by Dean (United States Patent 6,269,468, issued July 31, 2001). The rejection is respectfully traversed.

More specifically, the Examiner stated that Dean teaches designing an integrated circuit in accordance with a timing constraint, identifying critical and non-critical paths, and selectively optimizing the integrated circuit to reduce power consumption. (Office Action, p. 2). The Examiner concluded that Dean anticipates Applicants' invention recited in independent claims 1, 11, 14, and 17. (Office Action, p. 2). Applicants respectfully disagree.

Dean teaches describing a circuit design in a high-level definition language and synthesizing the circuit design by referencing a standard library database to define the gates to be used. (See Dean, col. 5, lines 11-20). The synthesized design is then processed to verify timing and power consumption. After implementing a traditional gate in the design, if it is determined that the timing of the circuit is not met, then the gate is replaced with a split input/output (I/O) version of the gate. (Dean, col. 5, lines 25-32). That is, Dean teaches replacing a circuit element with a split I/O circuit when the circuit element has a critical circuit path that fails a timing requirement of the circuit. (Dean, col. 6, claim 1, lines 25-30).

Dean, however, does not teach each and every element of Applicants' invention recited in claim 1. Namely, Dean does not teach or suggest "designing the integrated circuit in accordance with timing constraint data" and then "selectively optimizing the integrated circuit to reduce power consumption...." (See Applicants' claim 1). In contrast, Dean teaches a single timing-driven design process, where circuit elements

are replaced with modified versions if they fail a timing constraint. Dean does not teach or suggest a process whereby an integrated circuit is first designed in conformity with timing constraint data (e.g., a timing-driven process) and then optimized to reduce power consumption (e.g., a power-driven process), as recited in Applicants' claim 1.

The power reduction aspects taught in Dean must be taken in context with the entire methodology. In Dean, power reduction is achieved for those circuits that fail timing. That is, any power optimizations in Dean are part of a process of designing the circuit in accordance with timing requirements or constraints (i.e., part of a timing-driven process). In Dean, once the circuit design conforms to the timing requirements, no further optimizations are performed (i.e., there are no power optimization steps after timing is met at step 135 in FIG. 5 of Dean).

A single timing-driven process, as taught by Dean, does not teach or suggest a process where the integrated circuit is designed in accordance with timing constraint data and then optimized to reduce power consumption, as recited in Applicants' claim 1. "Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim." Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 221 USPQ 481, 485 (Fed. Cir. 1984). Since Dean does not teach a process whereby an integrated circuit is first designed in conformity with timing constraint data and then optimized to reduce power consumption, Dean does not teach each and every element of Applicants' claim 1.

Claim 11 recites, among other features, a computer readable medium for designing the integrated circuit in accordance with timing constraint data and selectively optimizing the integrated circuit to reduce power consumption. Claim 14 recites, among other features, a means for designing the integrated circuit in accordance with timing constraint data and a means for selectively optimizing the integrated circuit to reduce power consumption. Claim 17 recites, among other features, designing the integrated circuit in accordance with timing constraint data and selectively optimizing the integrated circuit to reduce power consumption. Each of these features are similar to those of claim 1 emphasized above. For the same reasons discussed above, Dean does not teach each and every element of Applicants' claims 11, 14, and 17.

Finally, claims 2, 4, 6-8, and 12-13, 15-16, and 18-20 depend, either directly or indirectly, from claims 1, 11, 14, and 17 and recite additional features therefor. Since Dean does not anticipate Applicants' invention as recited in claims 1, 11, 14, and 17, dependent claims 2, 4, 6-8, and 12-13, 15-16, and 18-20 are also not anticipated and are allowable. In view of the foregoing, Applicants contend that claims 1-2, 4, 6-8, and 11-20, are not anticipated by Dean and, as such, fully satisfy the requirements of 35 U.S.C. §102.

II. Rejection of Claims Under 35 U.S.C. §103

The Examiner rejected claims 3, 5, 9, and 10 as being unpatentable over Dean in view of Patra (United States patent 6,721,924, issued April 13, 2004). The rejection is respectfully traversed.

More specifically, the Examiner conceded that Dean does not teach placing first and second sets of logic with respect to a target device and routing connections of the first and second sets of logic paths. (Office Action, p. 4). The Examiner stated, however, that Patra teaches such features. The Examiner concluded that it would have been obvious to employ Patra's method of designing an integrated circuit with Deans method. (Office Action, p. 4). Applicants respectfully disagree.

Claims 3, 5, 9, and 10 depend, either directly or indirectly, from claim 1 and recite additional features therefor. The cited references, either singly or in any permissible combination, do not teach, suggest, or otherwise render obvious Applicants' invention recited in claim 1. Namely, the combination of Dean and Patra does not teach or suggest process whereby an integrated circuit is first designed in conformity with timing constraint data and then optimized to reduce power consumption. As discussed above in Section I, Dean does not teach or suggest such a two-stage design process. Patra teaches determining a set of objective parameters for a circuit and optimizing the values of such objective parameters based on noise constraints. Patra does not teach or suggest designing an integrated circuit in accordance with timing constraint data and then selectively optimizing the integrated circuit to reduce power consumption. Since neither Dean nor Patra teach or suggest the above-described elements of Applicants' claim 1, no conceivable combination of Dean and Patra renders obvious the invention of claim 1. Therefore, Applicants

contend that claims 3, 5, 9, and 10, which depend from claim 1, are patentable over the cited references and, as such, fully satisfy the requirements of 35 U.S.C. §103.

CONCLUSION

Thus, Applicants submit that none of the claims presently in the application are anticipated under the provisions of 35 U.S.C. § 102 or obvious under the provisions of 35 U.S.C. §103. Consequently, Applicants believe that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring any adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Kim Kanzaki at (408) 879-6149 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on November 2, 2005 .

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